

What is claimed is:

1 1. An evaluation wiring pattern construction for evaluating
2 reliability of a semiconductor device, said pattern construction
3 comprising a wiring configuration,
4 wherein a first wiring layer is connected to a second wiring
5 layer with a plurality of via plugs formed in an insulating layer
6 which is placed between said first wiring layer and said second
7 wiring layer,
8 wherein said first wiring layer and said second wiring layer
9 are made of metals having almost same specific resistances, and
10 wherein each different parasitic resistances is put to at
11 least one of said first wiring layer and said second wiring layer
12 connected to each of said plurality of via plugs.

1 2. An evaluation wiring pattern construction for evaluating
2 reliability of a semiconductor device, said pattern construction
3 comprising a wiring configuration,
4 wherein a first wiring layer is connected to a second wiring
5 layer with a plurality of via plugs formed in an insulating layer
6 which is placed between said first wiring layer and said second
7 wiring layer,
8 wherein said first wiring layer and said second wiring layer
9 are made of metals having almost same specific resistances, and
10 wherein said first wiring layer comprises a main wiring
11 portion in which current flows in common, and a plurality of branch
12 wiring portions each connected to a corresponding one of said
13 plurality of via plugs so that a current flows with different
14 resistance to a plurality of current paths respectively through

15 said plurality of via plugs from said main wiring portion in said
16 plurality of current paths through said plurality of via plugs.

1 3. The evaluation wiring pattern construction according to
2 claim 2, wherein said plurality of branch wiring portions each
3 connected to said corresponding one of said plurality of via plugs
4 in said first wiring layer are different from each other in length.

1 4. The evaluation wiring pattern construction according to
2 claim 3, wherein said plurality of said branch wiring portion are
3 formed to have stepwise great lengths from one side to another
4 side of said plurality of via plugs.

1 5. The evaluation wiring pattern construction according to
2 claim 2, wherein said plurality of branch wiring portions each
3 connected to a corresponding one of said plurality of via plugs
4 in said first wiring layer are different from each other in length.

1 6. The evaluation wiring pattern construction according to
2 claim 2, wherein said second wiring layer comprises a main wiring
3 portion in which current flows in common and a plurality of branch
4 wiring portions each connected to a corresponding one of said
5 plurality of via plugs so that a current flows with different
6 resistance to a plurality of current paths respectively through
7 said plurality of via plugs from said main wiring portion in said
8 plurality of current paths through said plurality of via plugs.

1 7. The evaluation wiring pattern construction according to
2 claim 1, wherein said plurality of via plugs is evenly spaced at

3 almost regular intervals in line.

1 8. The evaluation wiring pattern construction according to
2 claim 7, wherein said plurality of via plugs have same shape.

1 9. The evaluation wiring pattern construction according to
2 claim 2, wherein said plurality of via plugs is evenly spaced at
3 almost regular intervals in line.

1 10. The evaluation wiring pattern construction according to
2 claim 9, wherein said plurality of via plugs have same shape.

1 11. An evaluation method for evaluating reliability of a
2 semiconductor device, using an evaluation wiring pattern
3 construction comprising a wiring configuration in which a first
4 wiring layer is connected to a second wiring layer with a plurality
5 of via plugs formed in an insulating layer which is placed between
6 said first wiring layer and said second wiring layer, in which
7 said first wiring layer and said second wiring layer are made of
8 metals having almost same specific resistances, and in which each
9 different parasitic resistances is put to at least one of said
10 first wiring layer and said second wiring layer connected to each
11 of said plurality of via plugs,

12 wherein a time-variation of resistance is measured flowing
13 a constant current between a first wiring layer and a second wiring
14 layer.

1 12. An evaluation method for evaluating reliability of a
2 semiconductor device, using an evaluation wiring pattern

3 construction comprising a wiring configuration in which a first
4 wiring layer is connected to a second wiring layer with a plurality
5 of via plugs formed in an insulating layer which is placed between
6 said first wiring layer and said second wiring layer, in which
7 said first wiring layer and said second wiring layer are made of
8 metals having almost same specific resistances, and in which said
9 first wiring layer comprises a main wiring portion in which
10 current flows in common and a plurality of branch wiring portions
11 each connected to a corresponding one of said plurality of via
12 plugs so that a current flows with different resistance to a
13 plurality of current paths respectively through said plurality
14 of via plugs from said main wiring portion in said plurality of
15 current paths through said plurality of via plugs.

16 wherein a time-variation of resistance is measured flowing
17 a constant current between a first wiring layer and a second wiring
18 layer.

1 13. The evaluation wiring pattern construction according to
2 claim 12, wherein said plurality of branch wiring portions each
3 connected to a corresponding one of said plurality of via plugs
4 in said first wiring layer are different from each other in length.

1 14. The evaluation wiring pattern construction according to
2 claim 13, wherein a length of said branch wiring portion is formed
3 to have stepwise great lengths from one side to another side of
4 said plurality of via plugs.

1 15. A semiconductor device having an evaluation wiring pattern
2 construction for evaluating reliability of a semiconductor device,

3 said pattern construction comprising a wiring configuration,
4 wherein a first wiring layer is connected to a second wiring
5 layer with a plurality of via plugs formed in an insulating layer
6 which is placed between said first wiring layer and said second
7 wiring layer,

8 wherein said first wiring layer and said second wiring layer
9 are made of metals having almost same specific resistances, and

10 wherein each different parasitic resistances is put to at
11 least one of said first wiring layer and said second wiring layer
12 connected to each of said plurality of via plugs.

1 16. A semiconductor device having an evaluation wiring pattern
2 construction for evaluating reliability of a semiconductor device,
3 said pattern construction comprising a wiring configuration,

4 wherein a first wiring layer is connected to a second wiring
5 layer with a plurality of via plugs formed in an insulating layer
6 which is placed between said first wiring layer and said second
7 wiring layer,

8 wherein said first wiring layer and said second wiring layer
9 are made of metals having almost same specific resistances, and

10 wherein said first wiring layer comprises a main wiring
11 portion in which current flows in common and a plurality of branch
12 wiring portions each connected to a corresponding one of said
13 plurality of via plugs so that a current flows with different
14 resistance to a plurality of current paths respectively through
15 said plurality of via plugs from said main wiring portion in said
16 plurality of current paths through said plurality of via plugs.